

GeForce7050M-M

REV: 1.0A

PCB:15-V09-011010

BOM:81-605-V09110

MCP68PVNT Real S3

Components :718PCS

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25-AUDIO ALC861/660/662
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Signature

Date

Designer

Eli

07/09/2007

Layout

Susan/Angela

05/29/2007

Check

Approval



Elitegroup Computer Systems

Title

GeForce7050M-M

Size
B

Document Number

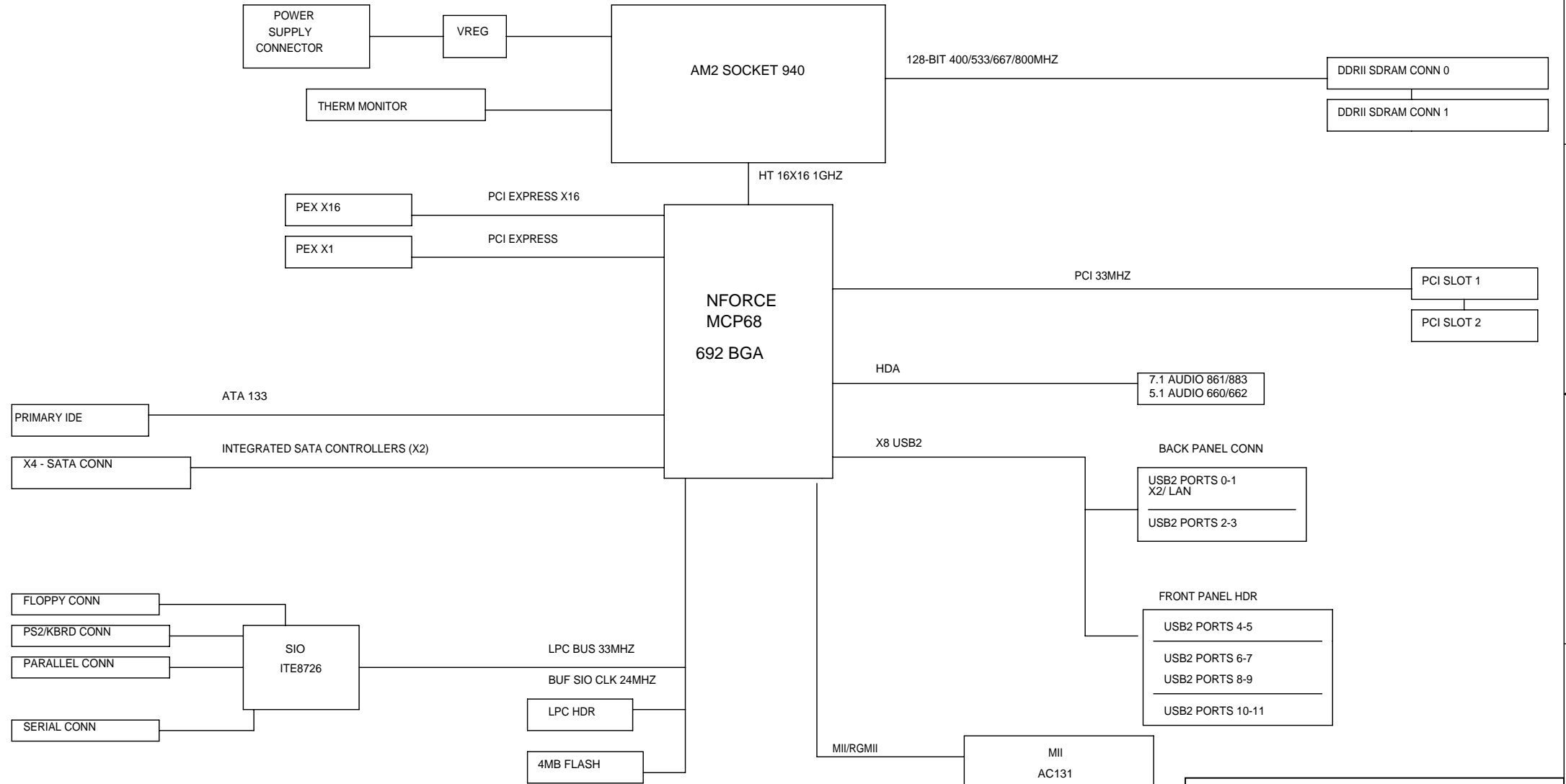
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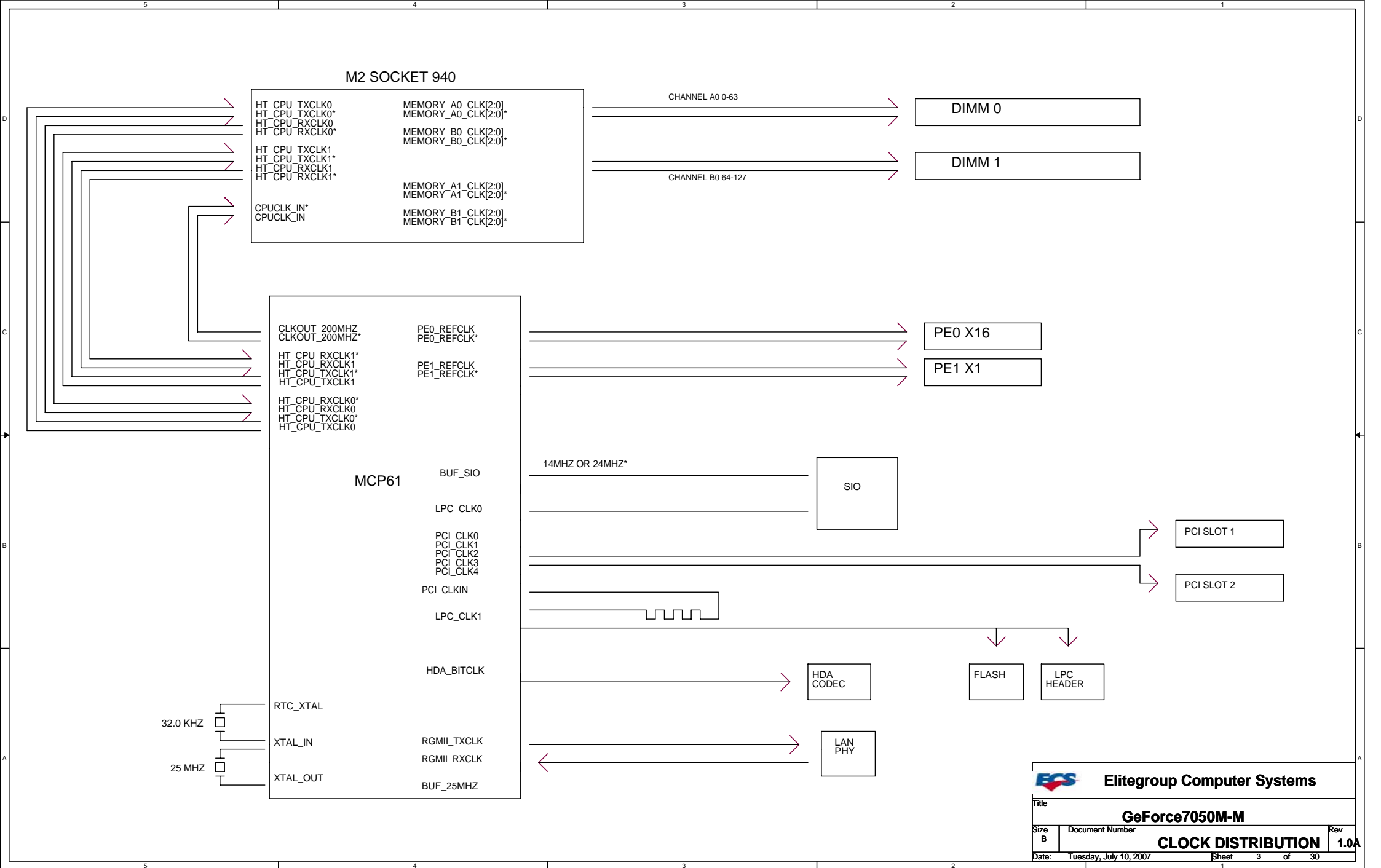
Rev
1.0A

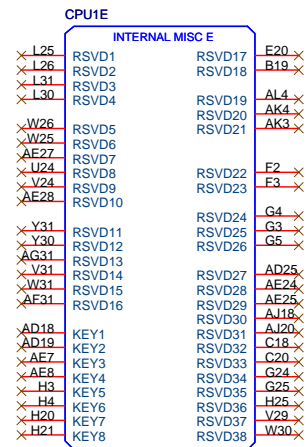
Date: Thursday, August 16, 2007

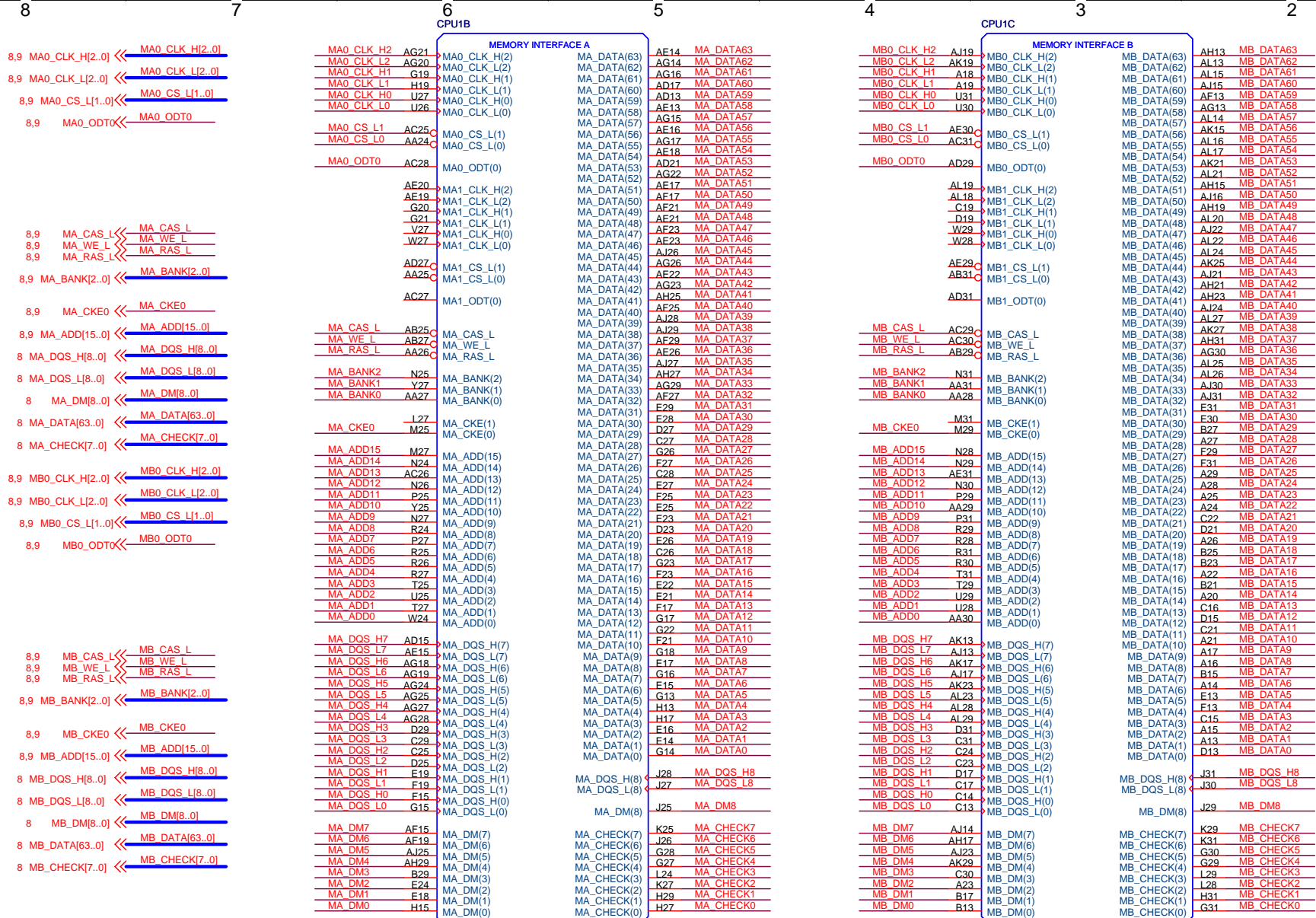
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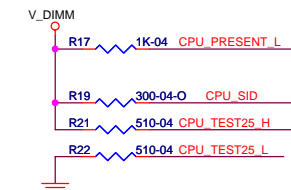
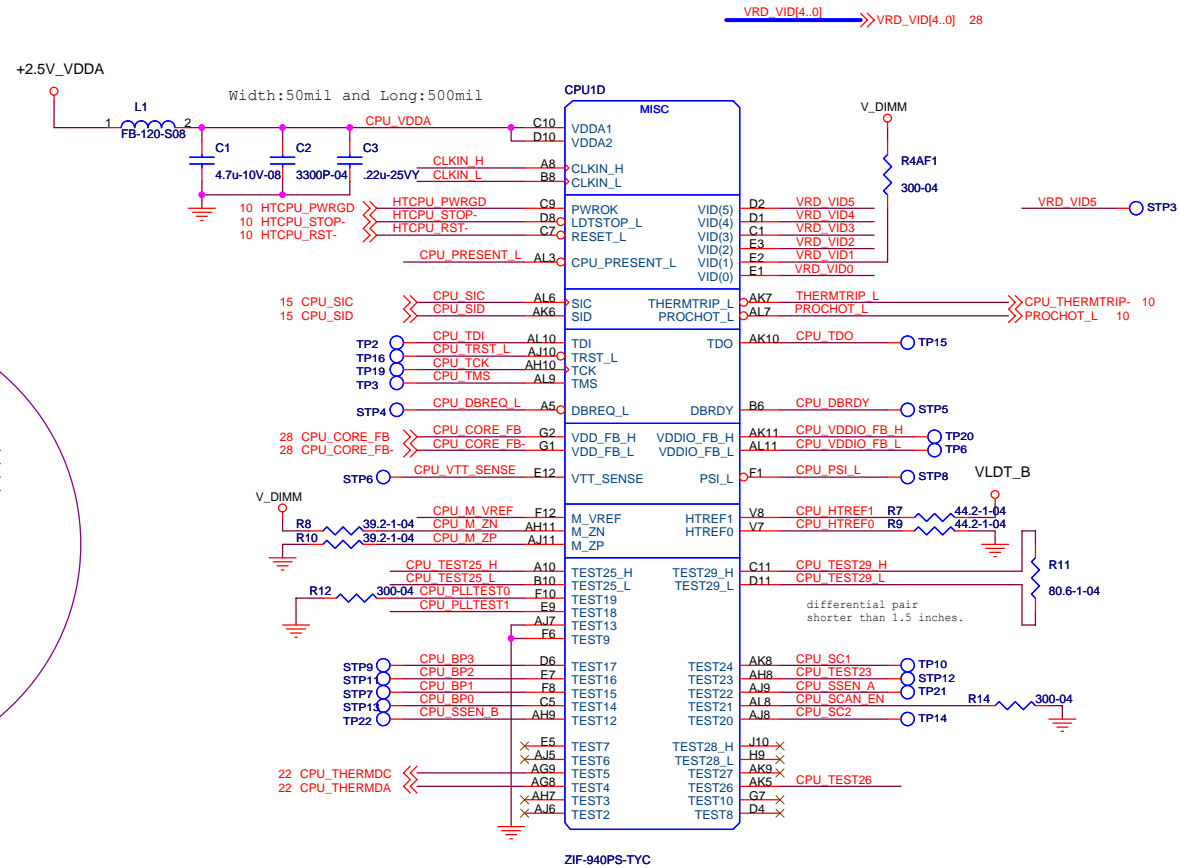
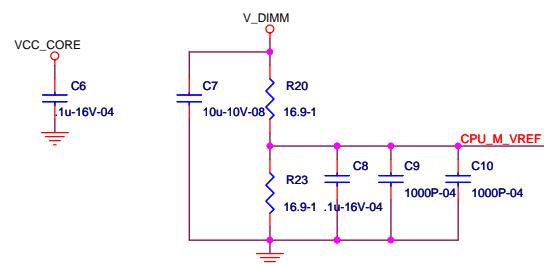
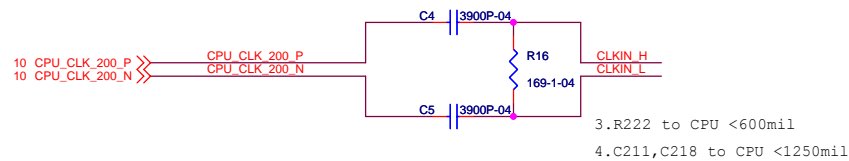
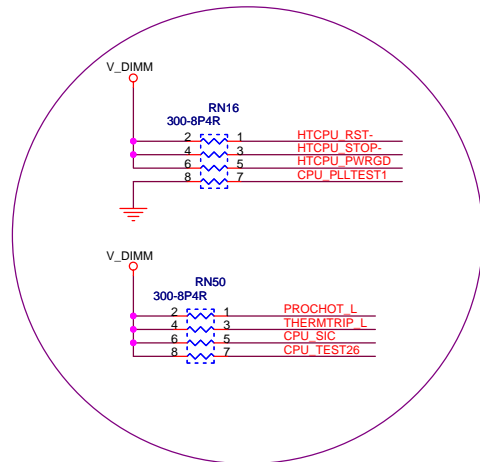
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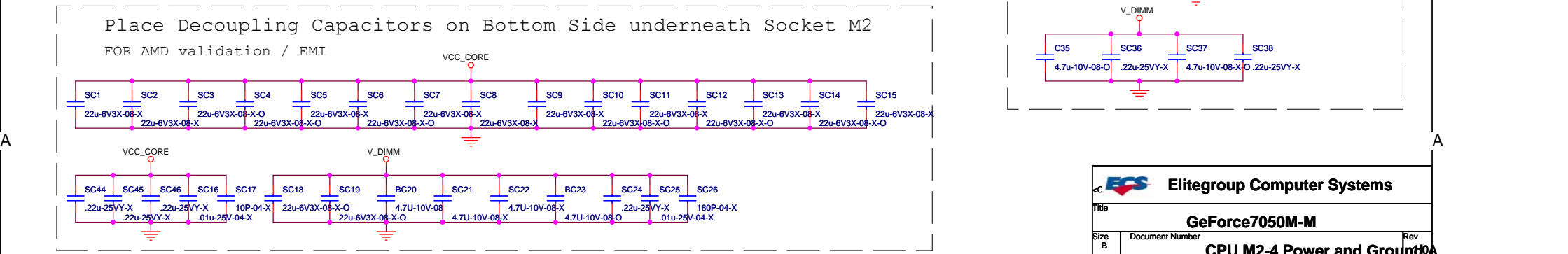
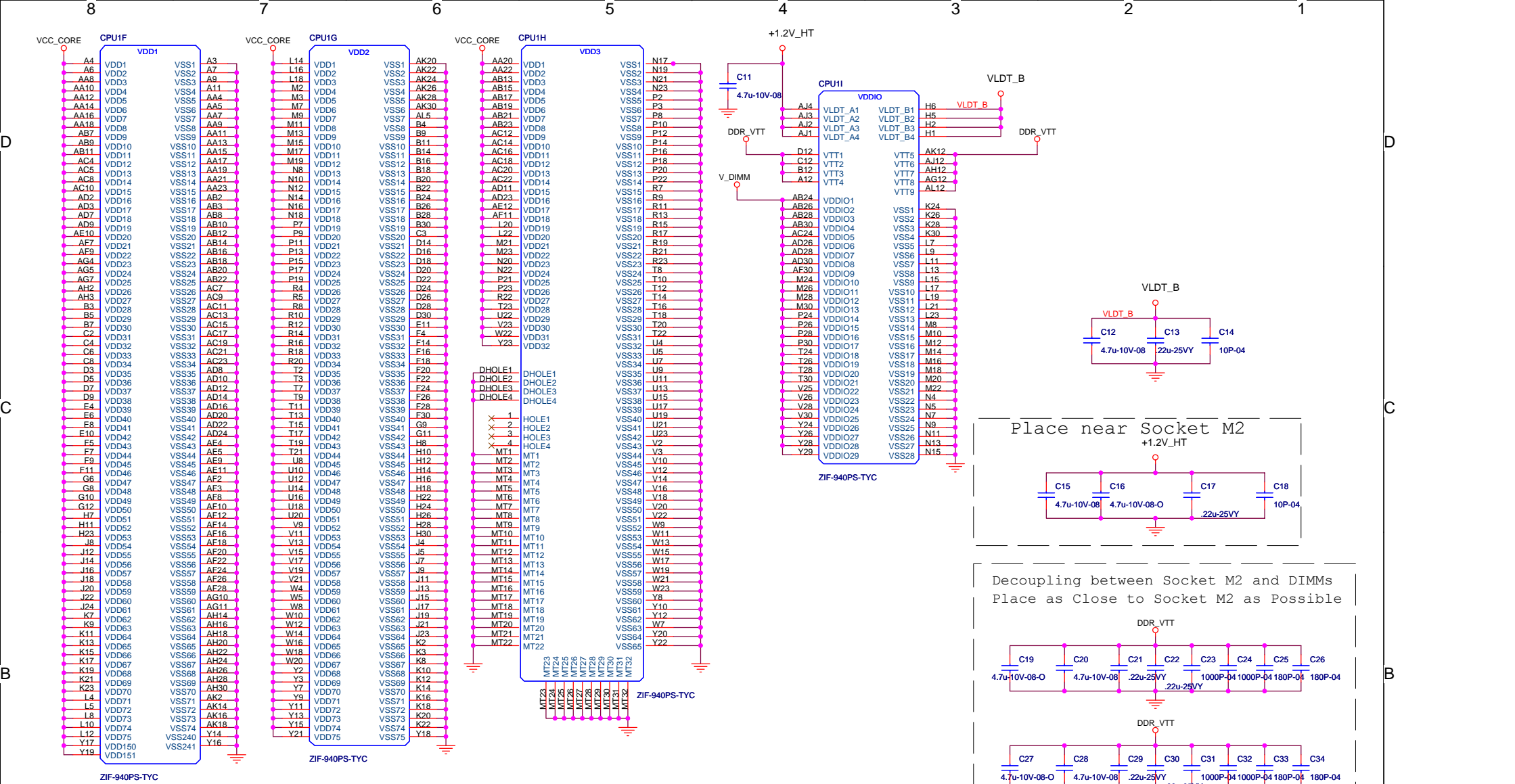


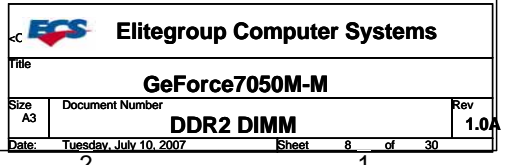


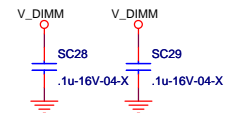
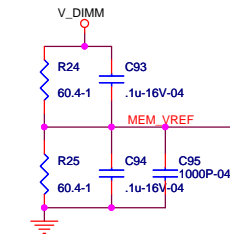
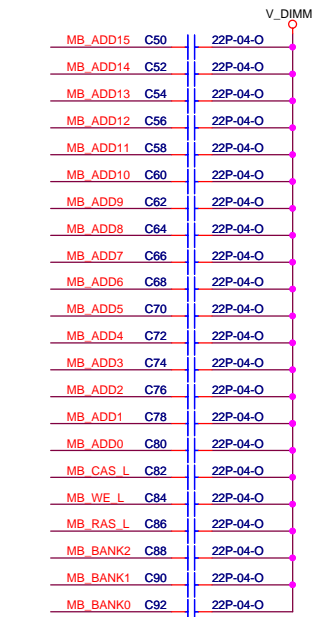
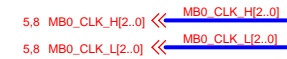
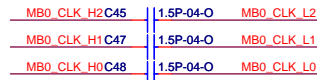
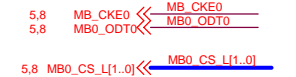
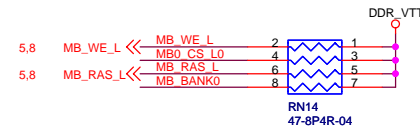
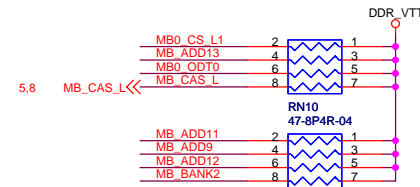
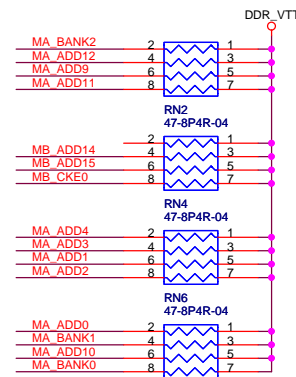
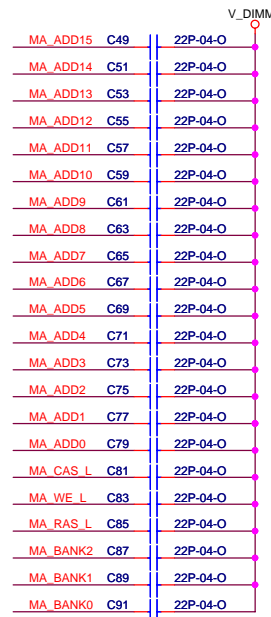
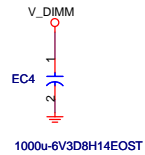
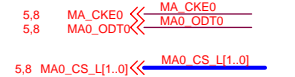
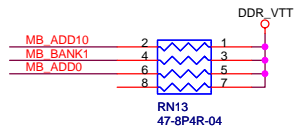
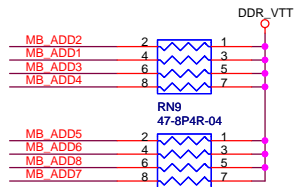
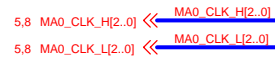
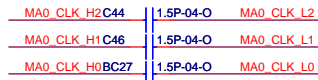
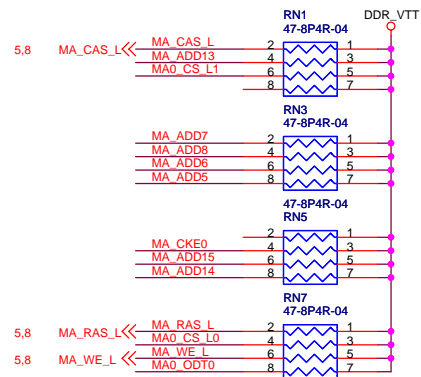






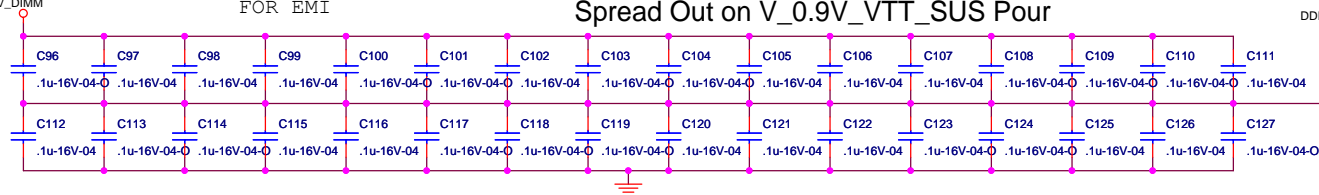


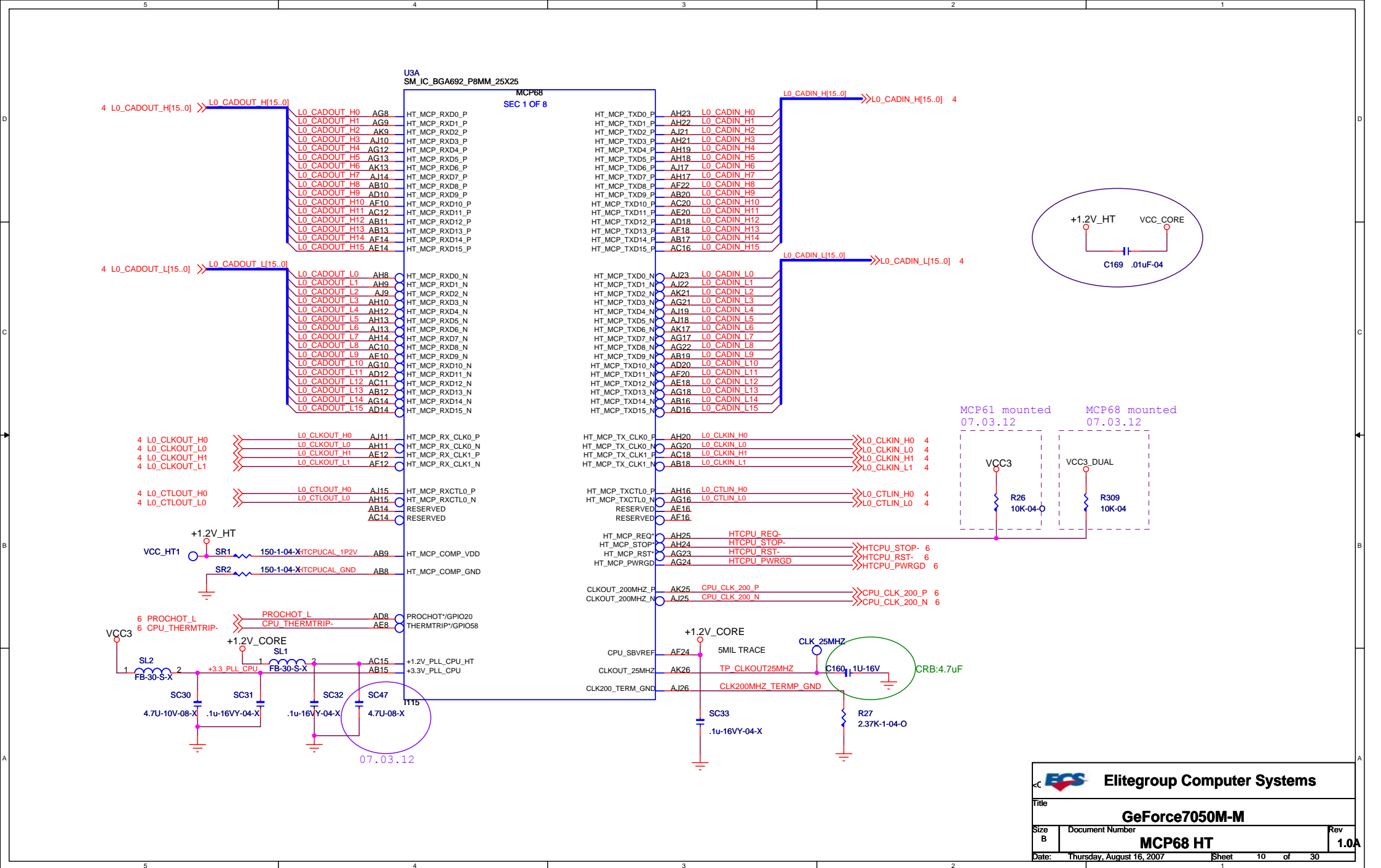




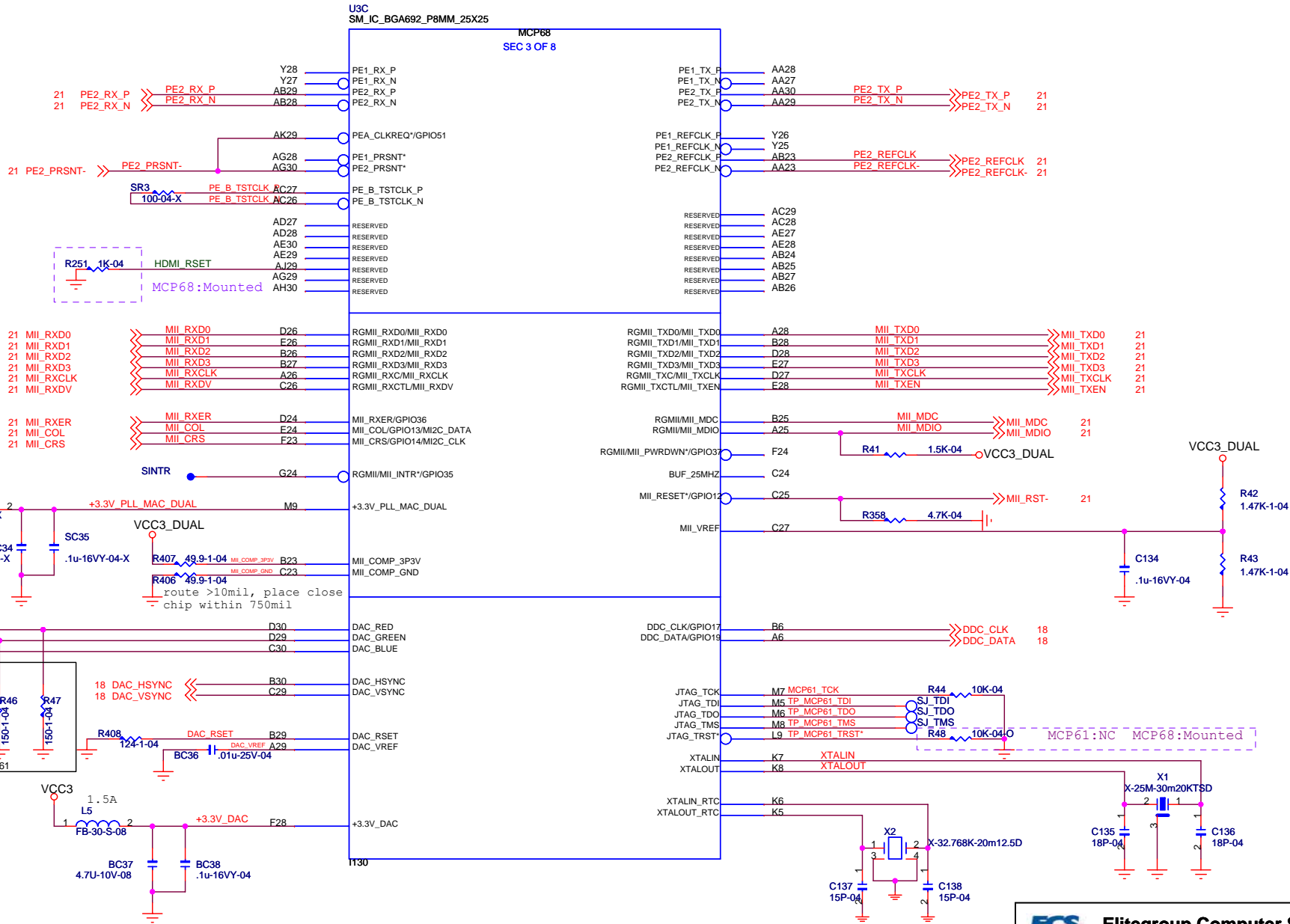
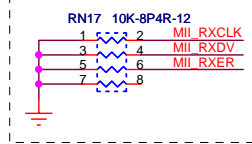
FOR EMI

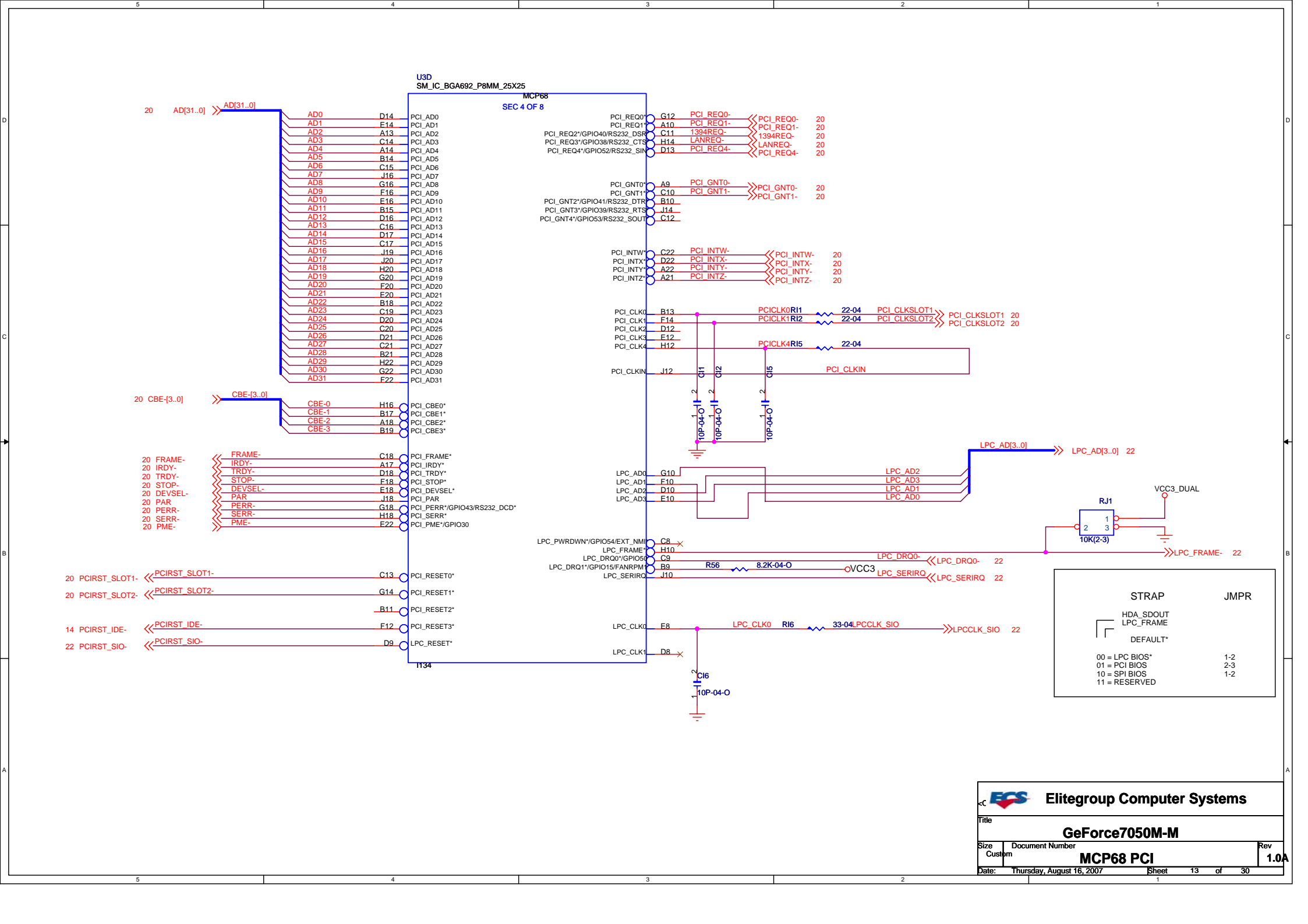
Spread Out on V_0.9V_VTT_SUS Pour

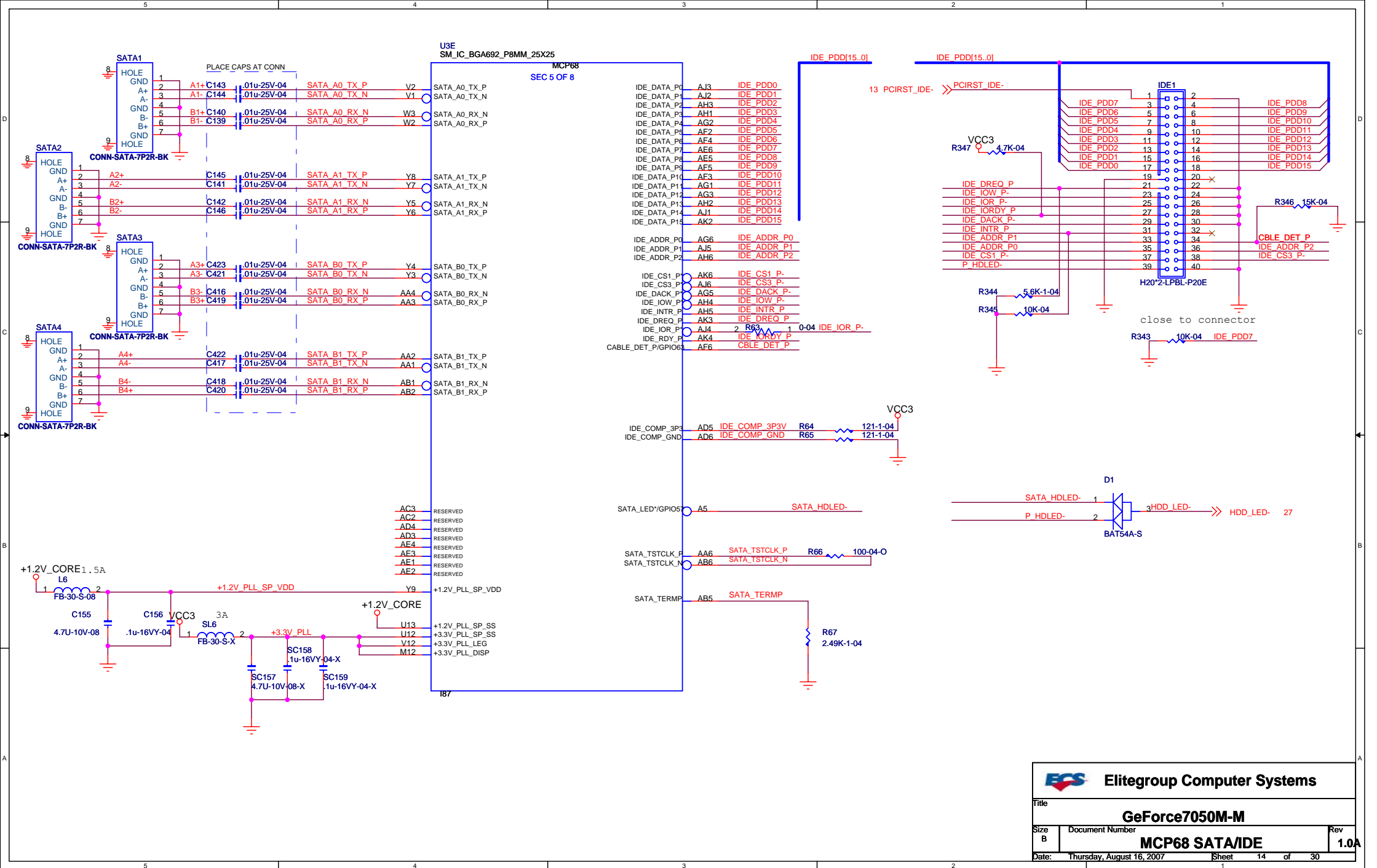




For enhance AC131 Driving





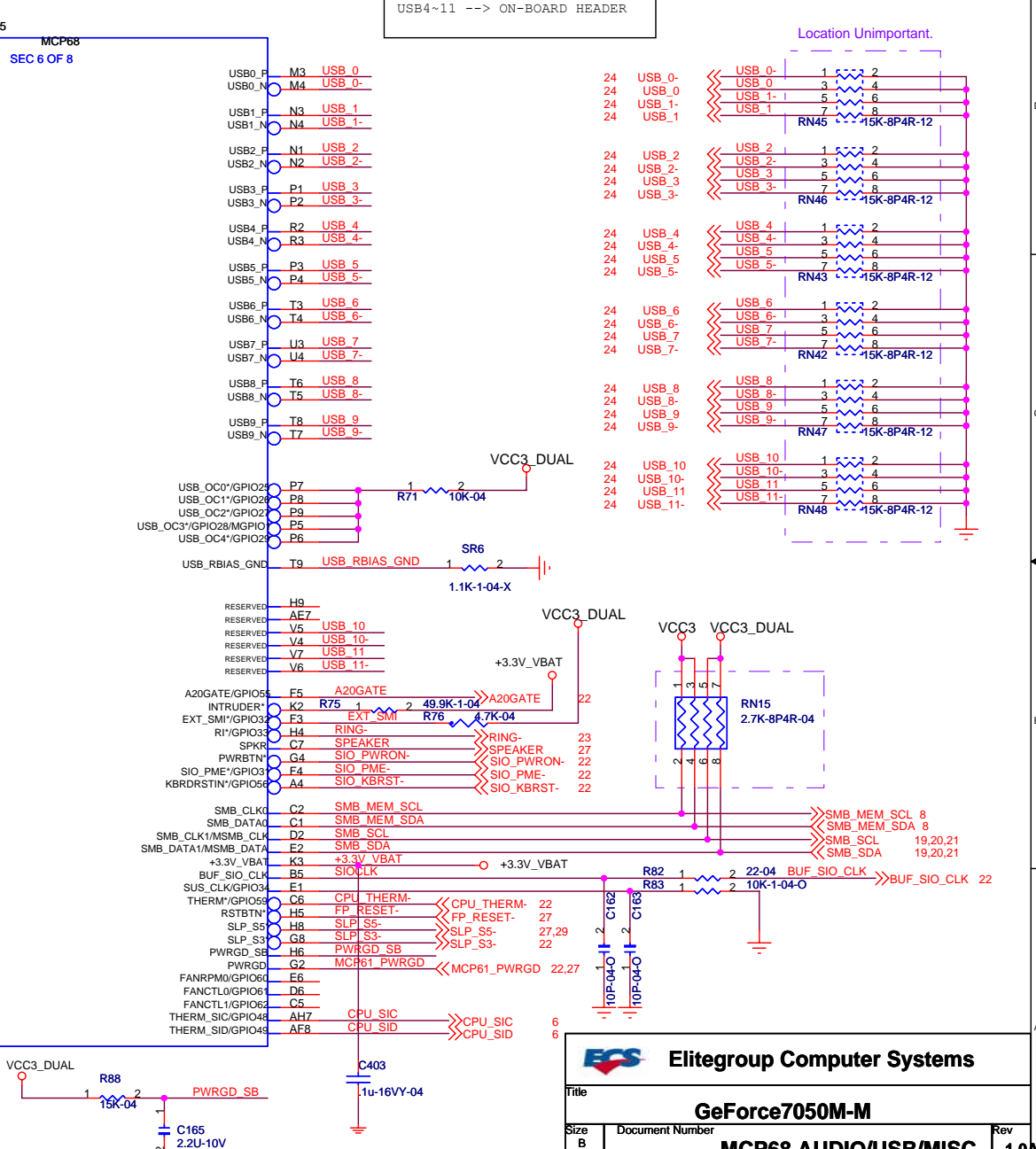
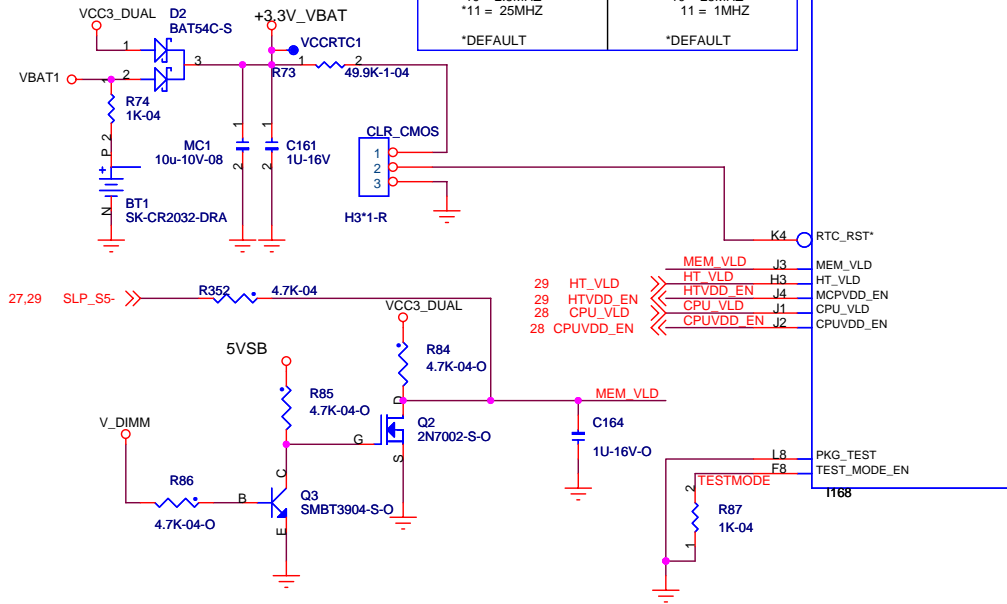
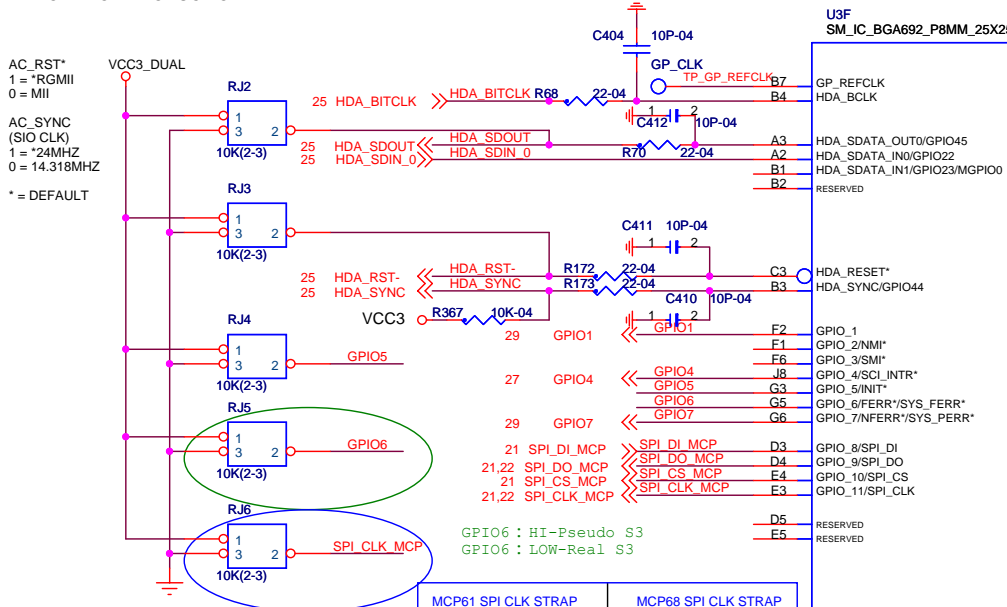


REMOVE FOR PRODUCTION

AC_RST*
1 = *RGMII
0 = MII


AC_SYNC
(SIO CLK)
1 = *24MHZ
0 = 14.318MHZ

* = DEFAULT



USB0~3 --> BACK CONNECTORS
USB4~11 --> ON-BOARD HEADER

Location Unimportant.

**Elitegroup Computer Systems**

Title

GeForce7050M-M

Size B

Document Number

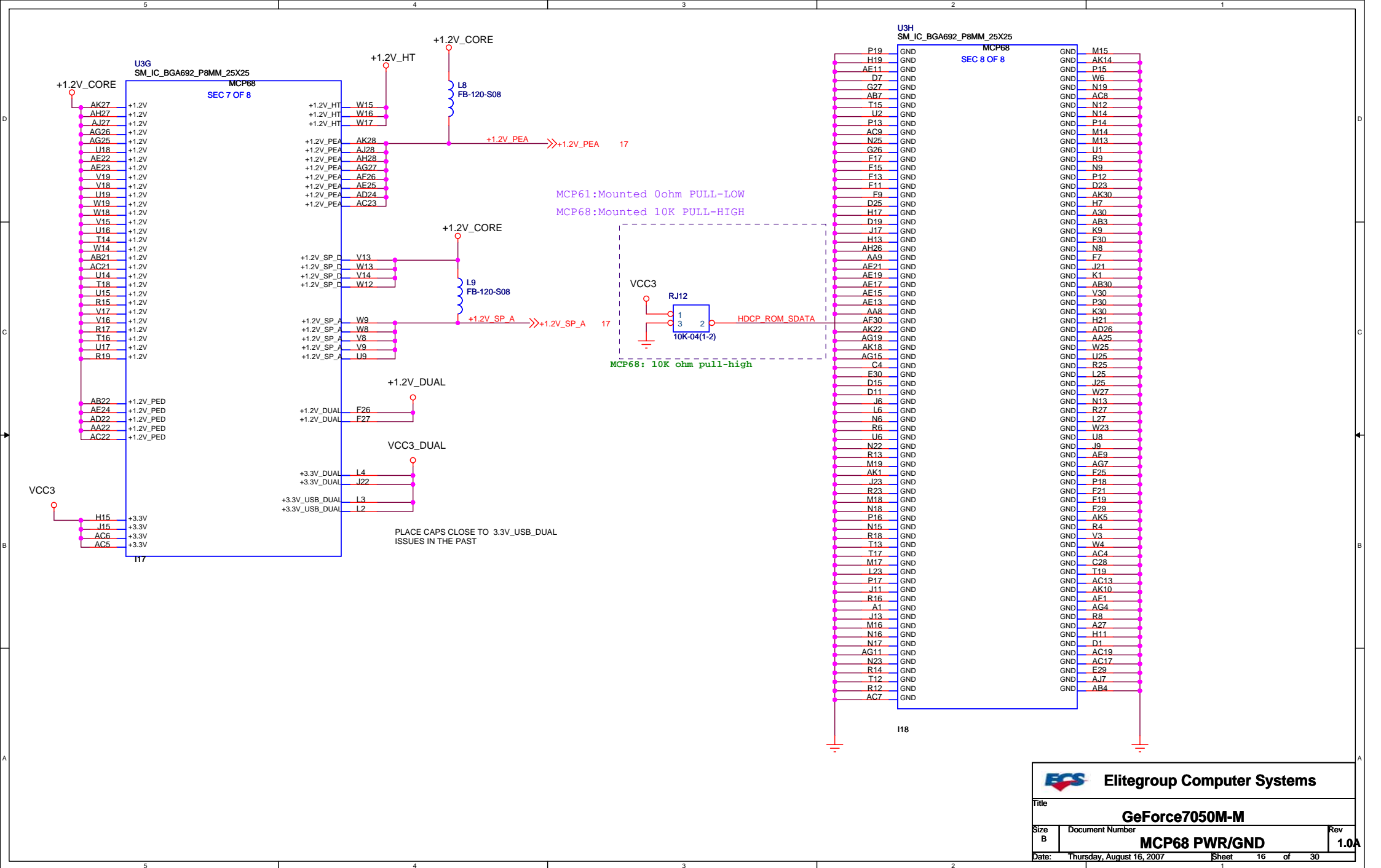
MCP68 AUDIO/USB/MISC

Rev

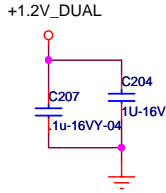
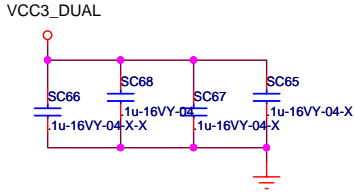
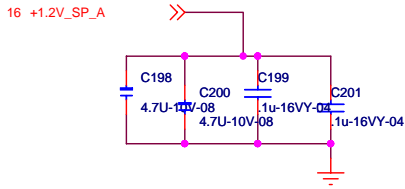
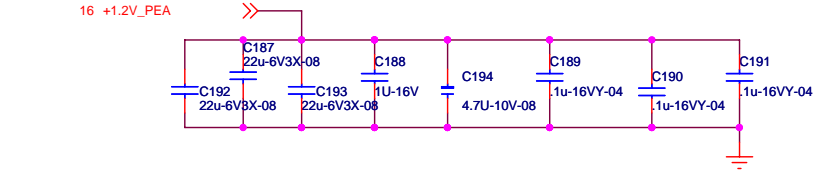
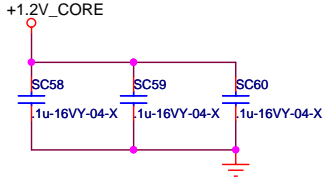
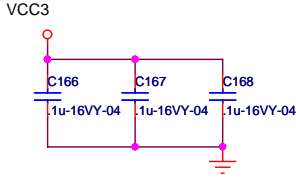
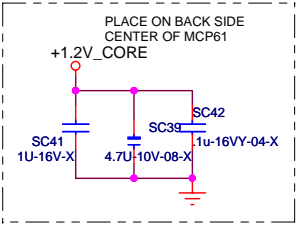
1.0A

Date: Thursday, August 16, 2007

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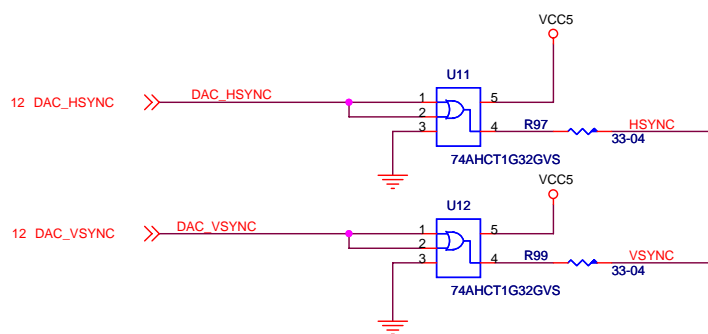
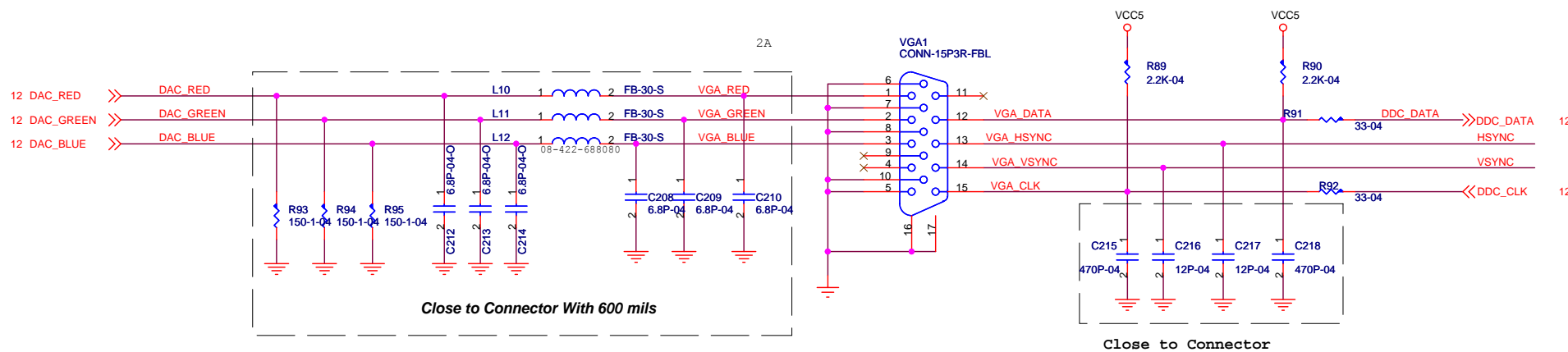


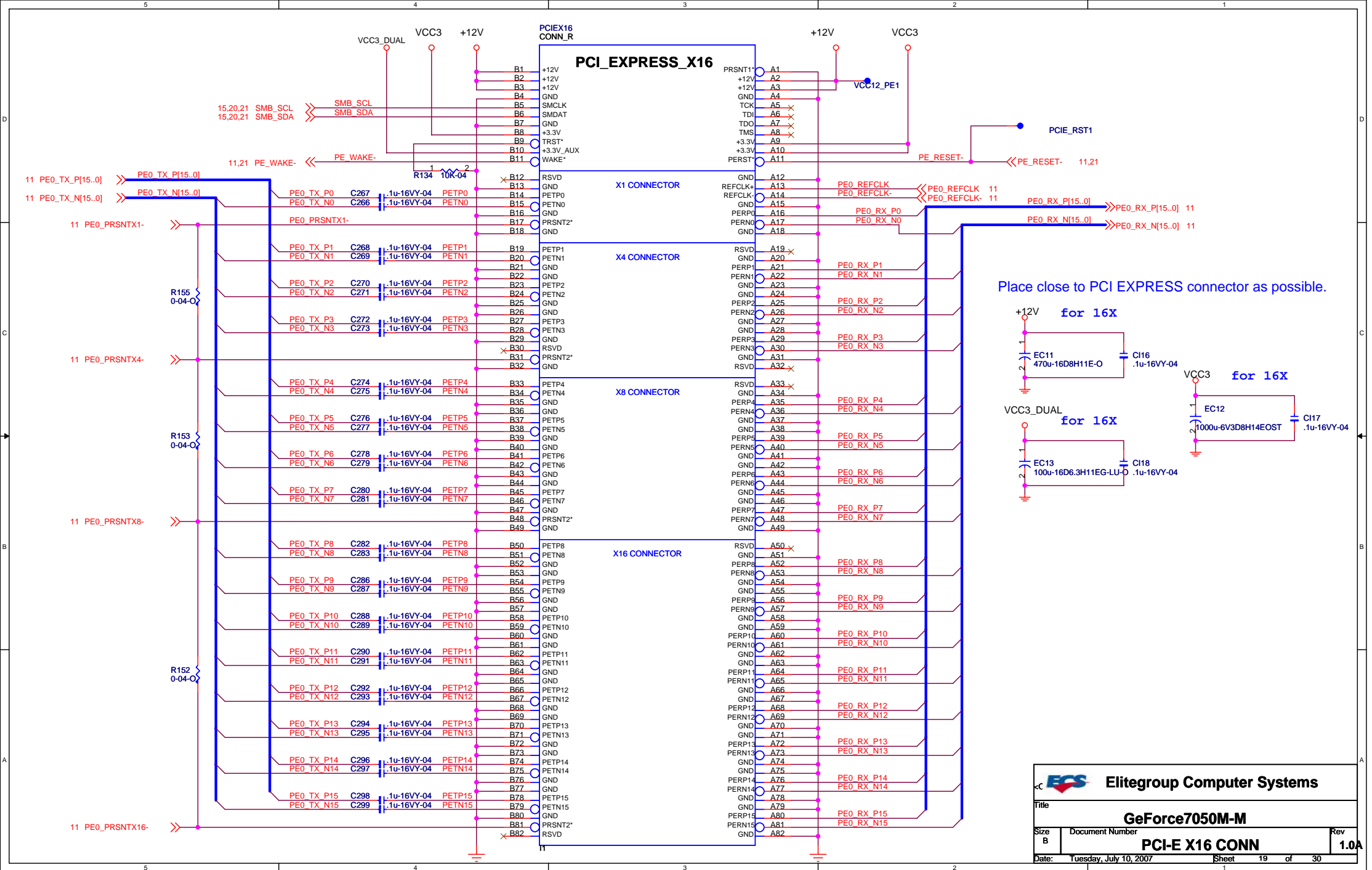
MCP61/8 DECOUPLING/EMI

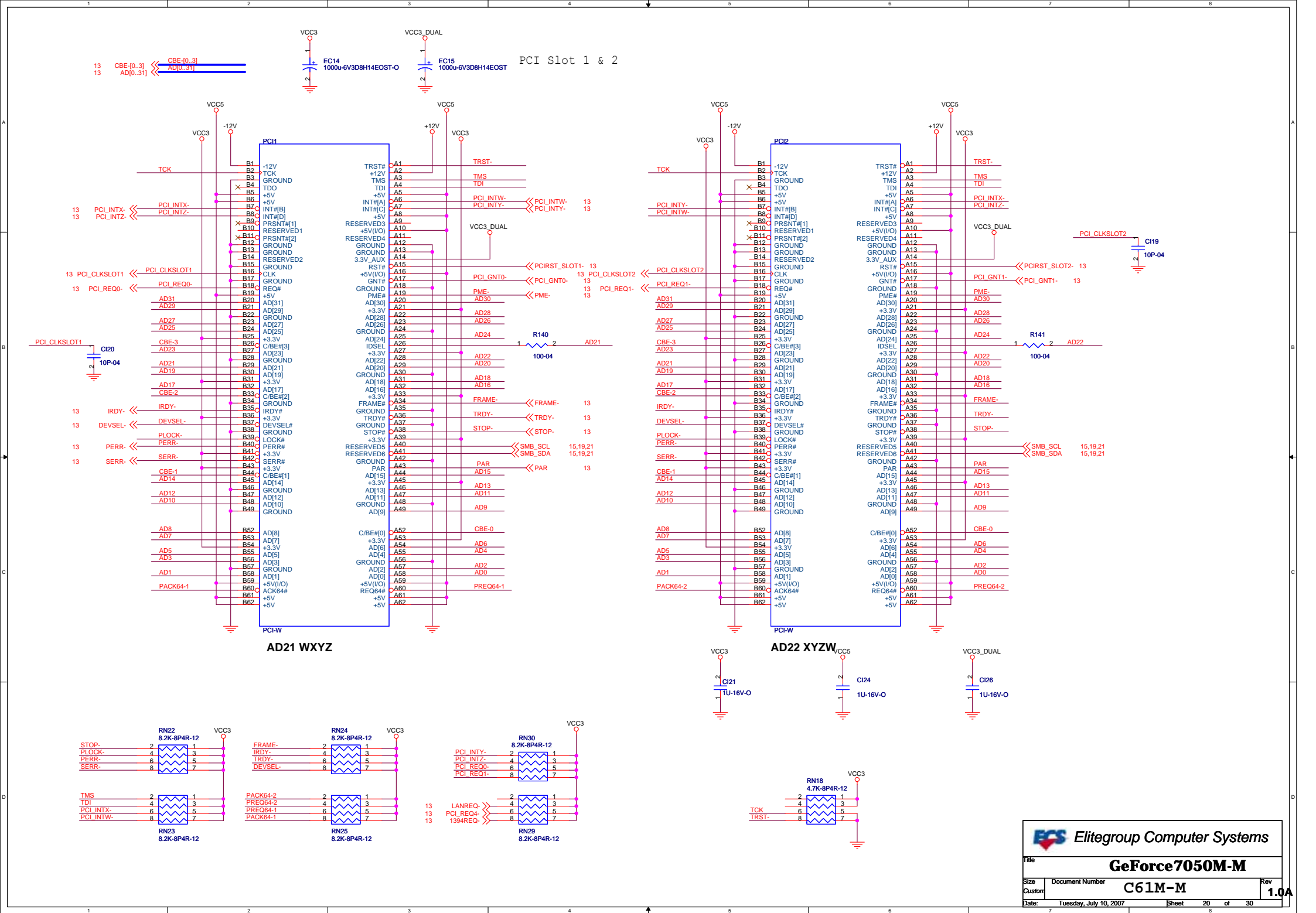


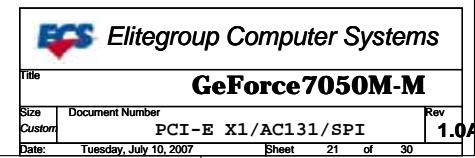
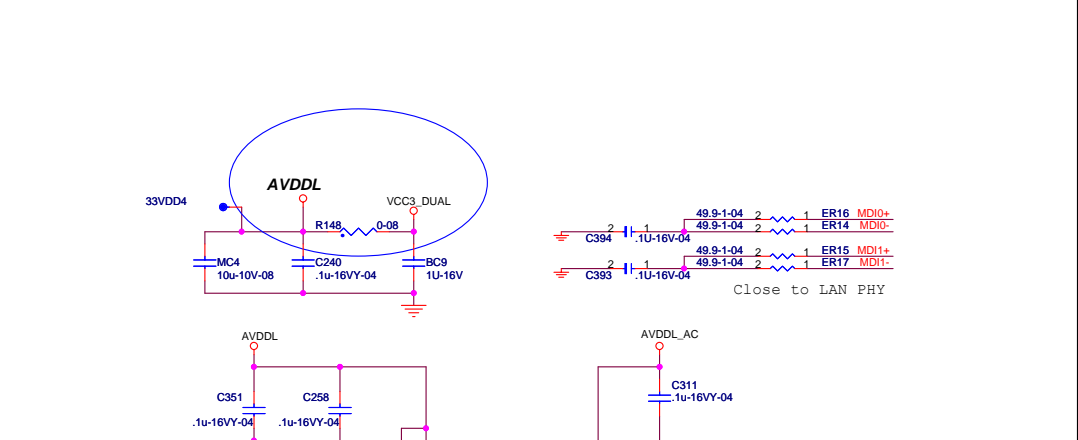
MCP61 INTERNAL PULL-UP/DWN'S

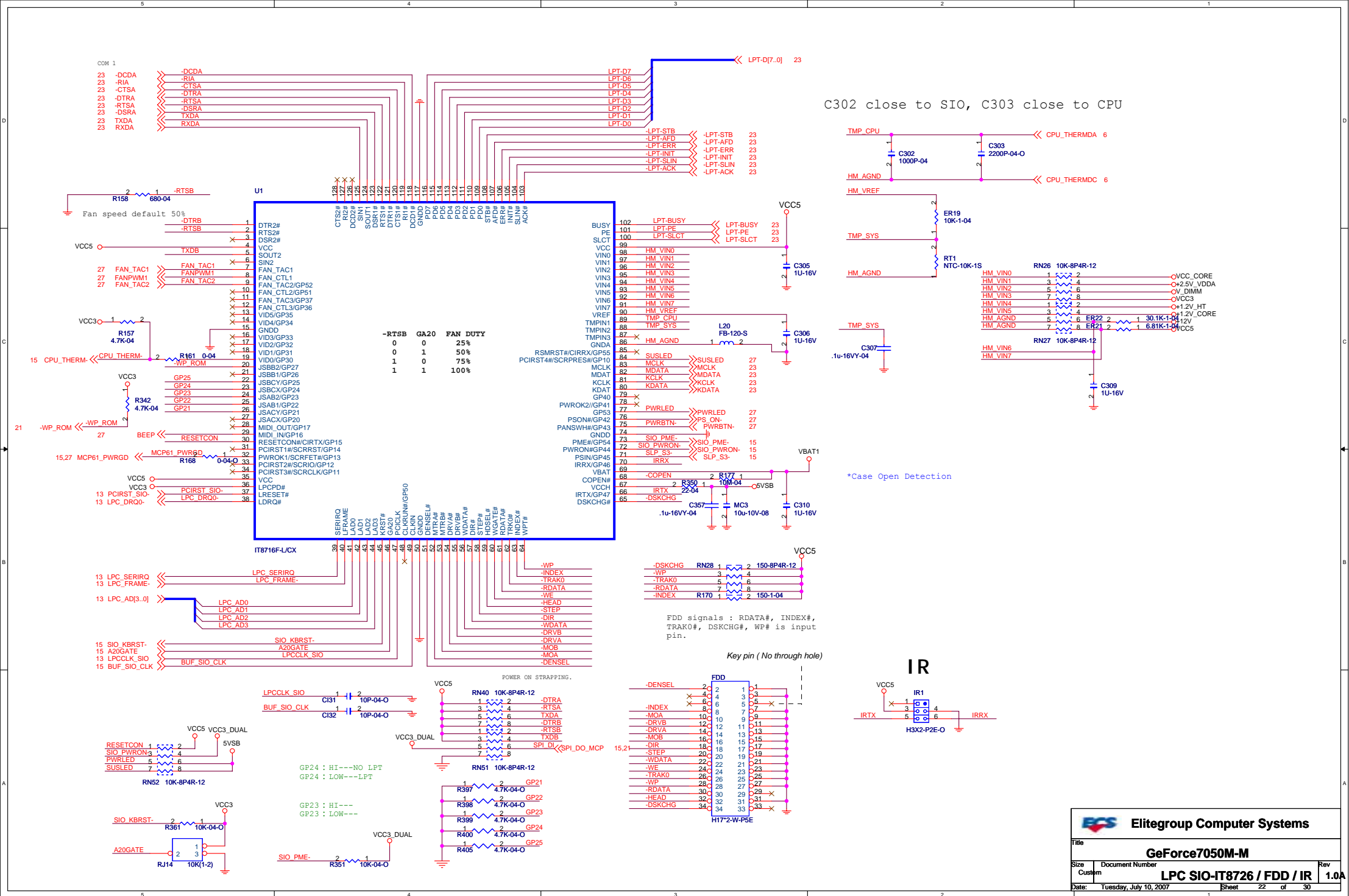
PE0_PRSNTX16* PE0_PRSNTX8*	10K PU TO 3.3V 10K PU TO 3.3V
PE1_PRSNT* PE2_PRSNT*	10K PU TO 3.3V 10K PU TO 3.3V
PE1_CLKREQ*	10K PU TO 3.3V
PCI_PME*/GPIO_30	8.2K PU TO 3.3V_DUAL
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 LPC_DRQ1/LPC_CS* LPC_DRQ0* LPC_SERIRQ	8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 10K PU TO 3.3V
HDA_SDATA_IN1/GPIO_23/MGPIO_0 HDA_SDATA_IN0/GPIO_22	10K PD TO GND 10K PD TO GND
JTAG_TMS JTAG_TRST* JTAG_TDI	10K PU TO 3.3V 10K PD TO GND 10K PU TO 3.3V
A20GATE PE_WAKE* EXT_SMIF/GPIO32 THERM/GPIO_59 KBRDRSTIN*/GPIO_58 RI*/GPIO_33 SIO_PME*/GPIO_31/MGPIO_2 PWRBTN* RSTBTN*	10K PU TO 3.3V 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V 10K PU TO 3.3V 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL

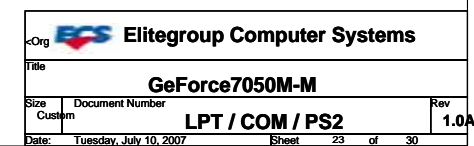
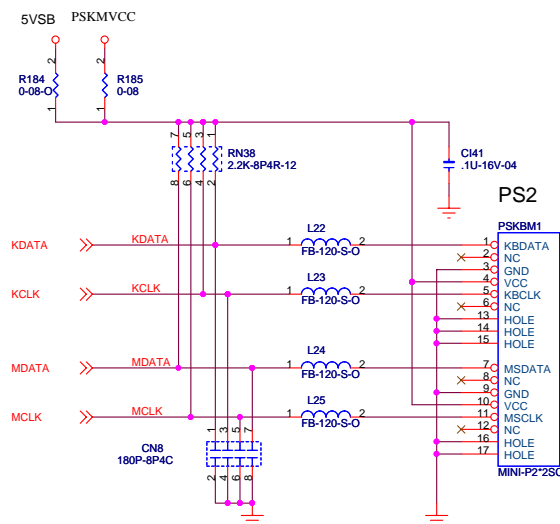
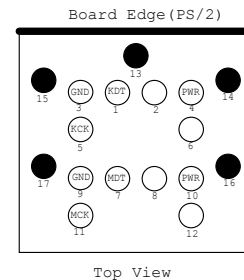


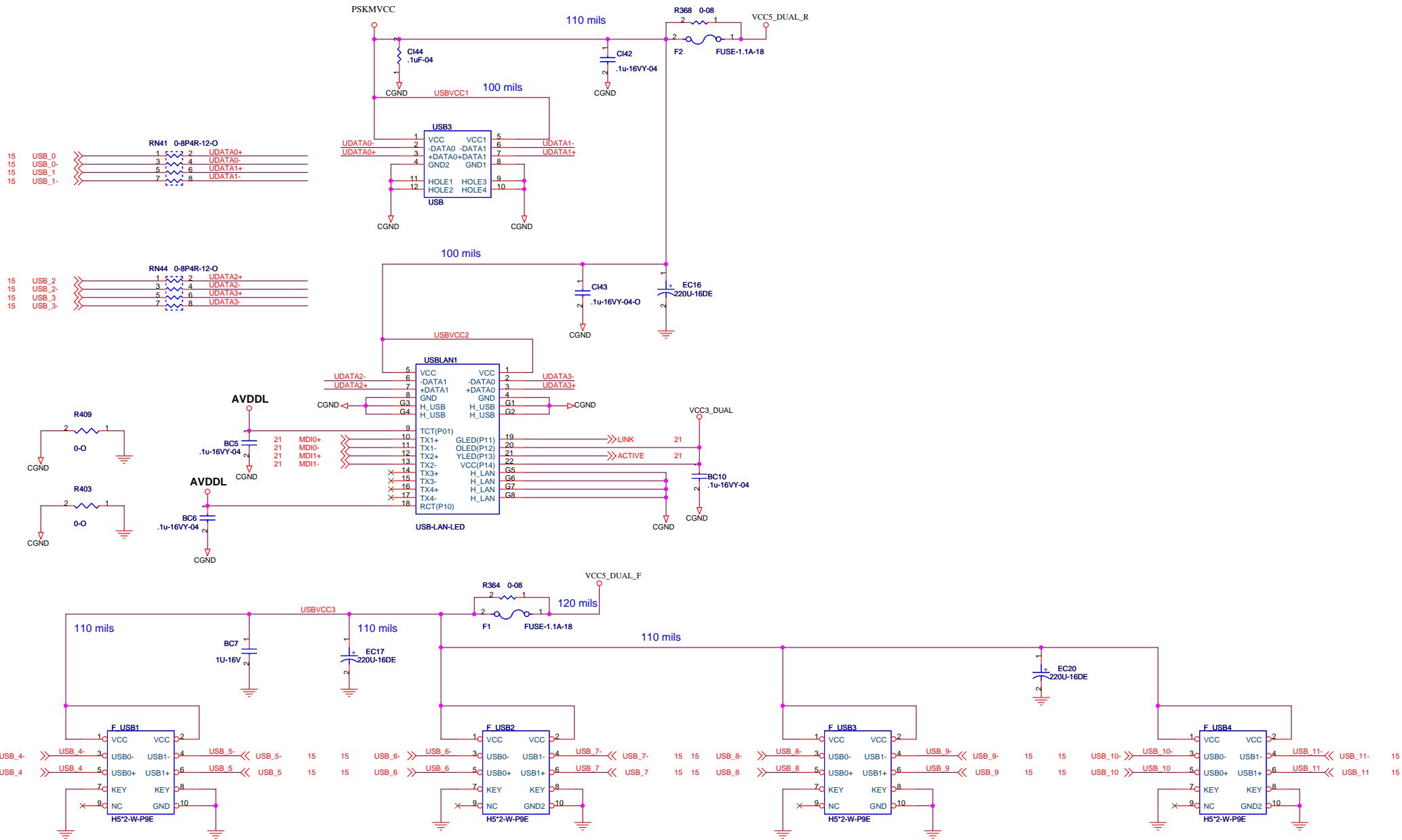






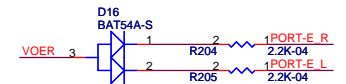
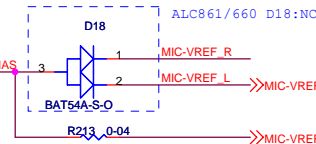
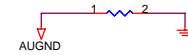
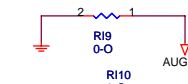
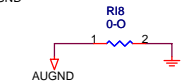
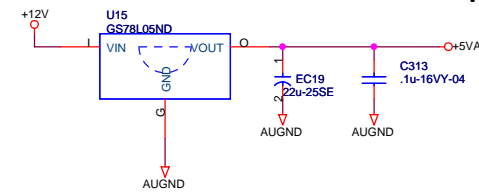






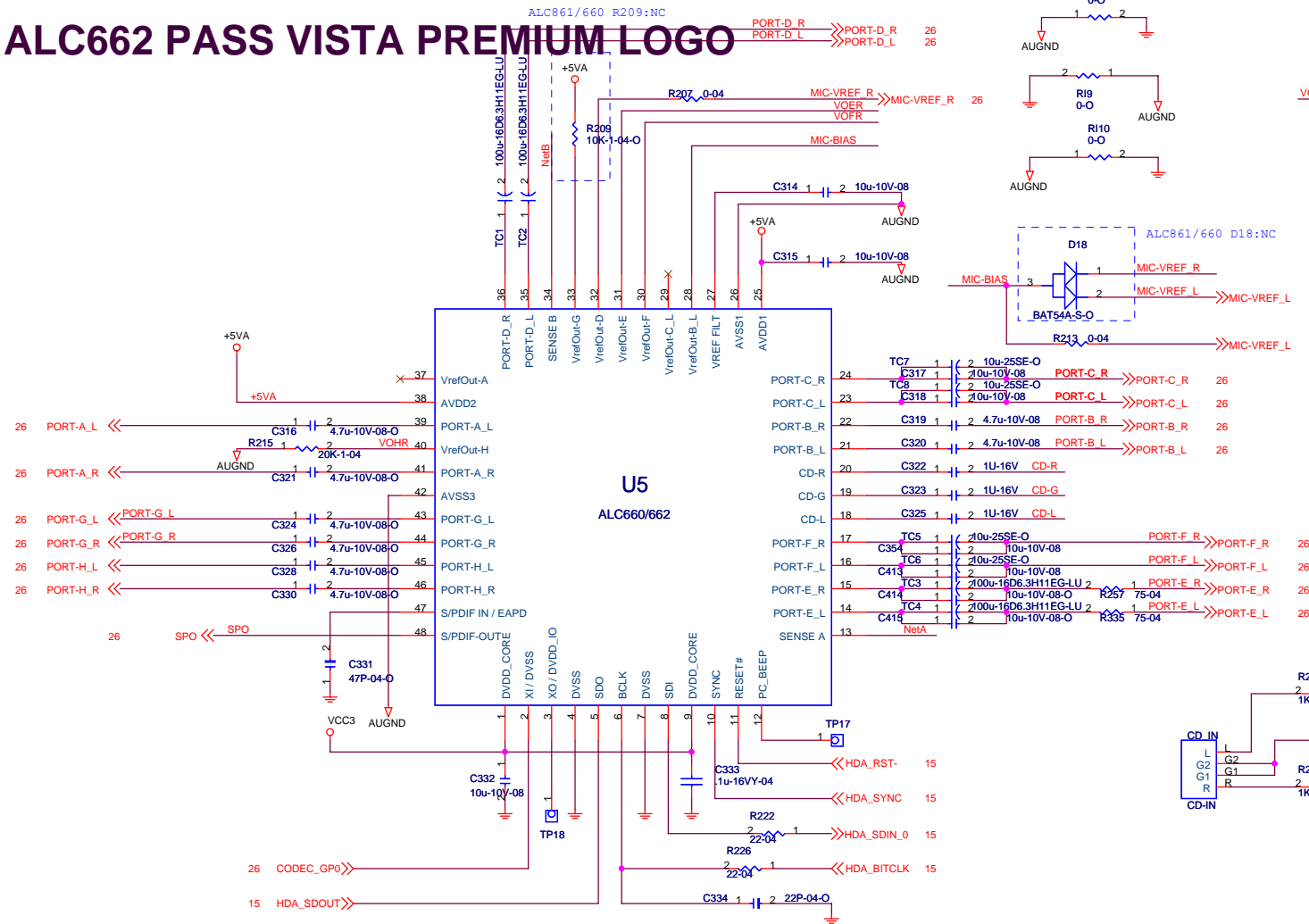
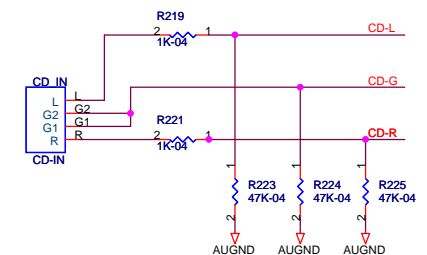
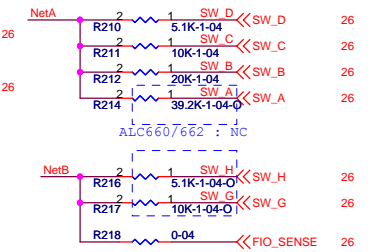
Improve the background noise of MIC boost

Verfout bias for stereo microphone.

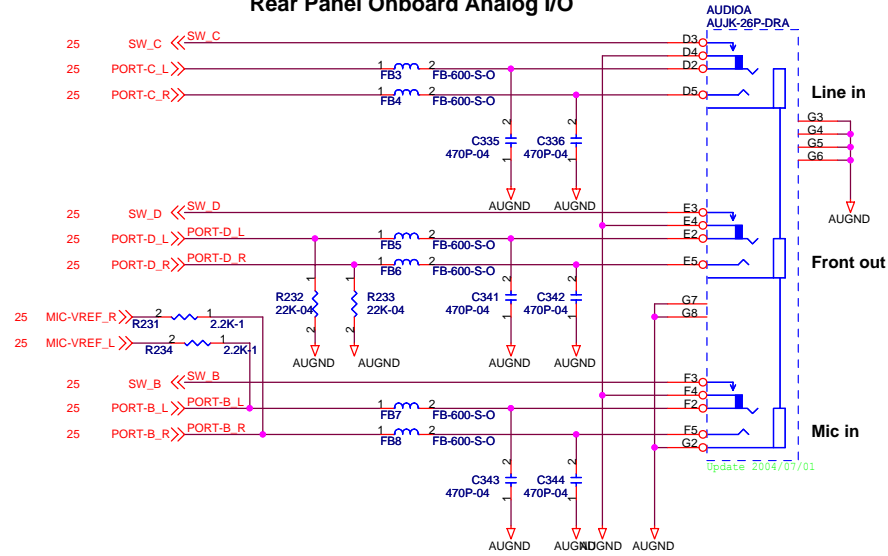


Place near Chip

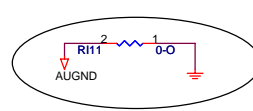
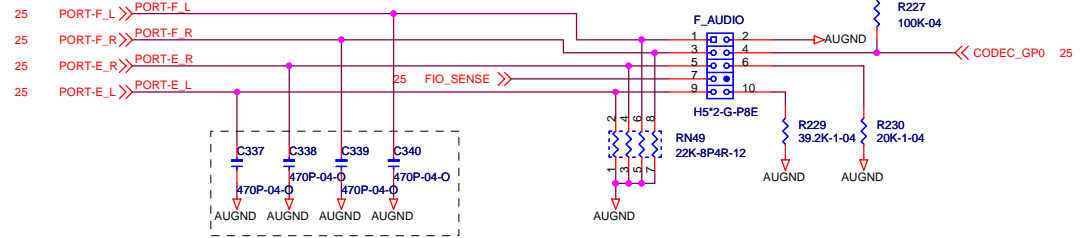
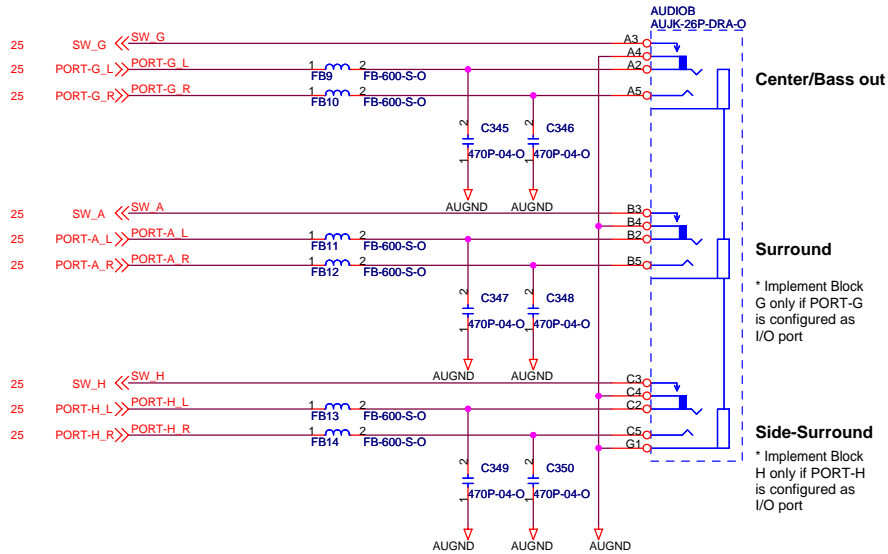
Resistors Networks



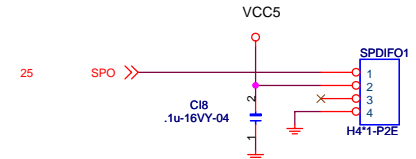
Rear Panel Onboard Analog I/O



Rear Panel (Optional Rear Audio Panel)



SPDIF Out



The schematic should consist with PINs define of I/O connector.

TOP VIEW

